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AI-Based Testing Frameworks for Next-Generation Semiconductor Devices

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Abstract

The semiconductor industry has been growing at a fast pace for the last decade. The ability to keep up with Moore's law and the ever-increasing chip complexity has become a tough challenge for manufacturers. The cost associated with testing these ICs has almost risen to that of the design. AI/ML is being actively explored as a solution to assist in almost every kind of issues arising in IC design and technology. IC testing plays a critical role in the production of reliable and functional chips. The increased complexity of the chips is leading to the introduction of new approaches and methods for improving existing and outdated methods. The test approach, automation, and tools used for 3D IC and FPGAs differ from the conventional ones used. The increase in chip complexity and the number of cores leads to a large power gouging. Test patterns for cores should be applied in a way that drastic changes to the current testing infrastructure and flows are avoided. Exploring opportunities for involving ML methods in different allied fields, such as screening equipment, failure cost reduction, optical DFT testing, etc. could also lead to improvements.

Machine-learning techniques have been adopted to help IC testing. However, ML application for fault detection and localization in the digital IC test domain still needs to be investigated. The approach towards the delineation of a fault model is presented first. The intelligent classification of faults is discussed in detail. It is followed by the description of design and defect models for ICs. Finally, an approach to developing AI-based testing frameworks for next-generation semiconductor devices is proposed. Test and Design-For-Testability (DFT) techniques for next-generation semiconductor devices, such as carbon nanotube-PMOS, 3D-ICs, and M-IGBTs, are emphasized. Exploring fault modeling techniques applicable to the modeling of faults in N-GaN HEMTs is important to support future DFT techniques and structure. Challenges in generating and applying conventional BIST methodology to the reconfigurable single-chip smart camera are discussed while proposing some solutions to these challenges.

Keywords: AI-based testing, testing frameworks, semiconductor devices, device testing automation, next-generation semiconductors, AI in electronics testing, smart testing systems, machine learning testing, automated chip testing, semiconductor AI tools

1. Introduction

The application of artificial intelligence (AI) in semiconductor device design, manufacture, testing, characterization, and reliability assessment is recently gaining much attention as a powerful and effective tool to meet the demands for maximized performance (both speed & power), lower geometries, lower costs, excellent quality, and reliability, enforcement of non-tariff trade barriers, etc. AI/ML techniques, like supervised learning (SL), semi-supervised learning (SSL), unsupervised learning (UL), reinforcement learning (RL), meta-learning (ML), random forests (RF), probabilistic graphical models (PGM), deep learning (DL), generative models (GM) including generative adversarial networks (GAN), and replica exchange algorithms, are applied in semiconductor design, testing, and characterization throughout the semiconductor (non-)automated design & test flows and systematic designs (dot designs, process design kits, and layout designs) of circuit blocks, pioneering models with unknown approximated closed-form transfer functions, discover trends in device parameters, physical effects, circuit architectures, etc. It is also comprehensively described how to incorporate AI/ML techniques in the classical IC design and testing flows [1]. To mitigate the data hurdle, a multi-alloy model-free meta-learning-based hybrid AI and numerical approach is proposed for passive analog circuits. The trained meta-RAJQ is the fastest known approach in the literature with reasonable accuracy cost trade-off. Both model-free and model-based AI methods are also applied to capture the efficiency and accuracy of a Nondominated Sorted Genetic Algorithm with a time-discrete simulation and those corresponding physical parameters. The new developments and a snapshot of the main methodologies in circuit design and test automation challenges for the aggressive 5 nm and below nodes are also expected to prompt researchers to contribute in these areas. The excellent IC reliability model+testing techniques and how AI/ML techniques can be utilized in them are also briefed. An overview of at-speed structured BIST for memory-based SOCs, along with the challenges and solutions, is also discussed.

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2. Overview of Semiconductor Devices

Various semiconductor devices are analyzed in this section, including the physical structure and working principles of tunnel field effect transistors (TFETs), two-dimensional materials and transistors, and memristors. The designs and characteristics of simple TFET circuits with tunnel diodes are given as a verification example for simulations using a closely tied framework.

With the continuous scaling down of MOSFETs, there has been a mounting concern over short-channel effects (SCEs) and leakage current, which lead to poor ON/OFF current ratio and restrictions of power supply scaling and circuit performance . As an alternative to planar MOSFETs, TFETs, which exploit the band-to-band tunneling (BTBT) mechanism, have drawn significant research interest because TFETs can achieve high ON-state current without the requirement of high supply voltage owing to the exponential dependence of tunneling current on the process or barrier controllability.

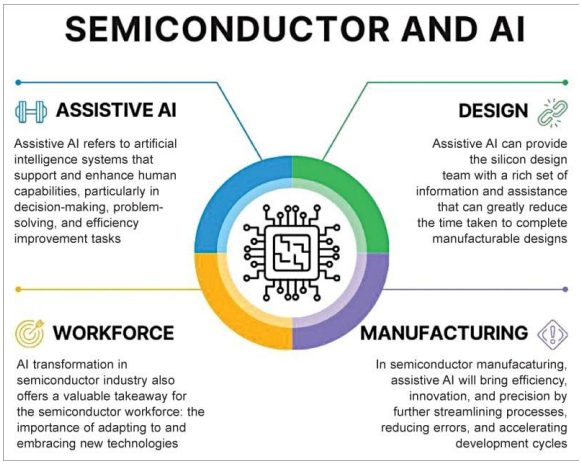

Fig : 1 Assistive AI - Semiconductor Design

Textured silicon is attractive due to its low processing cost and high volume for integratable photonic devices. Heterojunction TFETs based on crystalline textured silicon (CTS) and amorphous Silicon Oxide (a-SiO2) are reported for the first time. The TFET devices synthesized by ultra-thin layer transfer and deposition illustrate a bottom conduction band energy bowl and an internal accumulation region, facilitating the electrostatic control over carrier inversion and extraction. Transistors exhibit a high ON/(OFF+ subthreshold swing) current ratio of 3.23 * 10^8 (1400 times on-state current amplification) at 0.6 V, small variability of 19%, and subthreshold swing robust to the process variation with similar to 93.3% current reduction.

Two-dimensional (2D) materials and transistors are targeted for those applications which require high-speed, high-density, and low-power devices due to their ultra-thin body, low parasitic capacitance and power supply voltage, and robustness against SCE and off-state leakage. The 2D negative capacitance field effect transistors employ a ferroelectric 2D material as the dielectrics, breaking the Boltzmann limit on the sub-threshold swing, and exhibiting steep sub-threshold swing of 321 mV/decade, ultra-low leakage current of 0.106 nA/mu m, and excellent performance. The ferroelectric layer can be further horizontal stacked with other high-k dielectrics to be incorporated into current CMOS technology. Extension of 2D material transistors to novel functions is also explored, including multi-type logic gates, multi-transistor (MTL) inverters, chaotic signal generation and motor action.

Memristor (memory+resistor) is a two-terminal passive device with a nonlinear relationship between its current and the time integral of its voltage. Due to their multilevel resistance states and the highly controllable resistive switching, memristors have attracted tremendous research interest in developing RRAM (resistive random memory) as the embedded storage resource of future microprocessors. Memristor modeling is highly complex due to the stochastic, highly nonlinear, and non-ideal characteristics. For circuit simulation, a derived nonlinear interconnection of resistors with an order of magnitudes wider range is proposed to characterize memristors analytically.

3. Challenges in Semiconductor Testing

The design complexity of integrated circuits has grown as time-to-market periods have shortened. Decreased manufacturing geometries and increased transistor density have contributed to this escalation in complexity. For example, it is predicted that a single die in the 3 nm technology will consist of more than 100 billion transistors . Through reducing manufacturing costs and improving performance, semiconductor technology scaling has dramatically impacted the development of consumer electronics. Nevertheless, advanced semiconductor technology has introduced various challenges along with several opportunities, including yield loss, timing problems, low series resistance, limited power supply voltage headroom, substrate noise coupling, and increased leakage. These challenges are now common concerns for the semiconductor industry. As technology advancements push the miniaturization of semiconductor devices, maintaining their testability has grown in importance. Unfortunately, traditional structural test methods using test access ports are no longer effective. The challenges of testing integrated

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circuits have surged due to the rapid growth of the semiconductor test industry. As one of the most challenging tasks in integrated circuit manufacturing, semiconductor testing is a large design, verification, and analysis problem that employs various sophisticated techniques and enormous computational resources [2]. Contemporary semiconductor devices are frequently so advanced that the majority of testing is automated. As a result, failure analysis and testing of semiconductor devices have evolved into a complicated multi-disciplinary operation, involving physics, electrical engineering, computer science, and often mechanical engineering or material science. Consequently, conducting testing and failure analysis on semiconductor devices currently necessitates highly skilled professionals and the use of sophisticated instruments in a well-designed laboratory. The additional complexity associated with next-generation semiconductor devices requires more comprehensive test results, which should be gathered at higher speeds, especially for static tests. Additionally, devices need to be tested with greater accuracy, while different parameter distributions must be thoroughly analyzed to identify failure mechanisms. Furthermore, mask layout or its related dataset should be verified by reconstruction to achieve proper crosstalk and reliability, which often requires geometric manipulation at the nanometer scale. Adapting traditional test methods to meet these goals is doubly difficult due to the escalation of testing requirements on the one hand and the inaccessibility of devices on the other.

Eqn:1. Machine Learning Model for Fault Prediction

$$\hat{y} = f(\mathbf{x}; \boldsymbol{\theta})$$

- $\hat{y}$: Predicted output (e.g., faulty or not)
- $\mathbf{x}$: Input feature vector from device test data
- f: ML model (e.g., neural network, SVM)
- $\boldsymbol{\theta}$: Model parameters (weights)

4. Role of AI in Testing Frameworks

AI techniques can support all facets of software testing cycle, including review of SRS and design, test case generation, selection, prioritization, execution, reporting, and regression testing, and in finding faults in various artifacts. AI techniques help address a vast majority of the existing problems in testing activities, especially those that are tedious, time-consuming, monotonous, and require profound domain knowledge. AI techniques have been successfully deployed in developing tools that support many testing activities including test case generation and prioritization. There are many open questions and challenges that are yet to be addressed regarding the application of AI to software testing problems, which would remain a focus for future research work. AI techniques have been widely used in a wide area of computer science domain. AI testing has received careful consideration from academics and communities for guaranteeing the functionality and safety of AI models imbibed in intelligent systems [3].

For text-based and visualization-based testing, is there a white-box testing technique that would deliver better results than the equivalent black-box technique? Test oracle problem is a companion of every researcher and practitioner working in the field of software testing. Despite continuous attempts to mitigate the problem of the test oracle, researchers have been able to solve this problem for a static subset of SUT's. As soon as the dynamic traits of the SUT start to display, the previous test oracle derived for the SUT starts to lose effectiveness. AI techniques have been employed to cope with this dynamism.

5. Machine Learning Techniques for Testing

Testing complexity is on the rise due to the rapid growth of the main-driven semiconductor sector. This makes it more difficult for testers to choose the right test setup and parameters for new devices. Recently developed AI-based testing frameworks can efficiently evaluate next-generation devices. Expert generator algorithms suggest various test setups and parameters, whereas simulator-based stochastic optimization identifies optimum setups and parameters [1].

For SOI FinFETS and multi-gate devices, recent AI predictors exhibiting prediction capabilities comparable to advanced SPICE simulators have made on-chip analog testing feasible. Predicted values can be used to calculate a test set of values. A classifier is used to filter opportunities needing expert examination, and results are presented compellingly. With growing design complexity and finite manufacturing yields, defects in couple or entire blocks render their area and power procured unnecessarily. AI-based classification and global area loss analytics effectively contain excessive area consumption.

Additionally, AI tools can enhance traditional methods for fault attribute generation and fault and error classification. Combining these tools can further tailor the generated profiles with respect to new faults and errors isolated by

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theory. New AI test methods can be compared with traditional ones at each applied design maturity level. Industry-survey results on the capabilities of AI techniques for test and reliability are presented, along with their technical challenges and state-of-the-art developments. The survey covers architectures, algorithms, data sources, and application fields.

5.1. Supervised Learning Approaches

In a supervised approach, the learning process can be divided into two phases: a learning phase and a testing phase. During the learning phase, a training set composed of both the device inputs and the expected outputs is used to teach the algorithm. During the testing phase, the trained model is evaluated using a separate test set. The most common supervised ML approaches are random forests, support vector machines, and artificial neural networks.

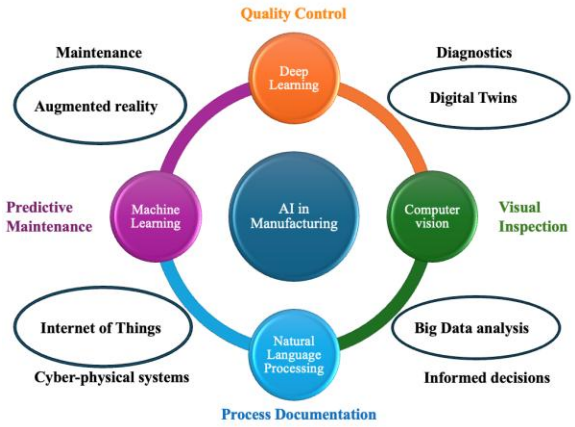

Fig : 2 Artificial Intelligence and Machine Learning

By predicting the output of a power amplifier (PA) and training a single-layer feed-forward neural network (SLFFNN), good predictive performance can be achieved even in the presence of noise and inter-domain design space. Careful tuning of hyperparameters can yield an average correlation coefficient of 0.985 for the validation set and less than 4.2 dB relative error between the predicted output and the expected output for all samples of the test set. Key insights about the expected output can be derived from a trained second-layer ELU activation function. In addition, by employing an ensemble method with inputs mapped to a 200, 243 filter size, good outputs can be obtained, even with tight margins of 0.055 mA, as compared to the ideal expected output of 60 × 2.5 mA.

A gated recurrent unit-based time-series forecasting and analysis framework for complex dynamic systems. A decoupled architecture employing GRU and LSTM networks to model the dynamic system where non-linear interactions exist across spatial dimensions can capture complex patterns in the data streams and have demonstrated remarkable predictive performance. A GRU-based forecasting model architecture is employed for five downstream tasks, which are compared against several benchmarks over several performance metrics. A novel post-prediction approach and protocol to compute reconstruction error for open-set anomaly detection task can trigger off-the-shelf anomaly detection algorithms to improve detection performance on unseen anomalies.

5.2. Unsupervised Learning Techniques

Machine learning is a field of computer science that employs statistical techniques to enable computers to learn from data. It is often integrated into systems where explicit programming would be challenging or impossible. A machine learning approach for engineering applications include case-based reasoning systems, neural networks, genetic algorithms, support vector machines, clustering methods, control sense and response gains, and inference-based systems or expert systems. In recent years, some applications have emerged through the massive use of machine learning techniques in different sectors such as the identification of uncharacteristic regions in WAFER MAP using deep learning approaches, general time-series forecasting methods using LSTM and attention models, and guidance on how to debug a semiconductor process using machine learning techniques.

In AGGREGATE WAFER MAP DEFECT CLASSIFICATION using Deep Learning approach, predefined patterns are generated for individual defects. Optical SEM images of the defects are also captured and classified by a Convolutional Neural Network based classifier. The network is made deeper through successful trials on various defects to achieve a 98% classification accuracy. Each defect class has a pattern and a corresponding optical SEM image. Model-based approaches use predefined patterns. After applying model-based methods, if a defective pixel is found, verification routines capture SEM images of that region. The data acquisition is not only time consuming but also needs skilled engineers to distinguish the pixel's defect class as each defect class may contain a different process. The unsuitable conditions for memory use by these techniques emerge as it is difficult to discover new defect classes and the regenerative nature of the defects in semiconductor processes [4].

Class-Specific Autoencoder is proposed to reconstruct the input sample as the representation learns the degree of abnormalities. Data-Specific Variational Deep One-Class Classifier is suggested to minimize the reconstruction error by applying regularization in learning parameters. A new representation is learned using a conditional generative

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network and one-class sinless classification is accomplished. To the best of the authors' knowledge, this work is the first to propose a one-similar class defect for wafer map classification by combining both GAN and one-class classification techniques.

5.3. Reinforcement Learning in Testing

Integrating the latest computing architectures in verification might open a new exciting path for accelerating the testing of next-generation semiconductor devices and cutting overall power and thermal budgets. Accelerators built using GPUs and other high-compute capabilities are perfect candidates to test deep-learning accelerators and frameworks commonly used in designing new chips. There are already significant computing resources dedicated to simulation and emulation but dedicated units for thorough testing are needed

Eqn 2 : Loss Function (Binary Cross Entropy for Fault Classification)

$$\mathcal{L} = -\frac{1}{N}\sum_{i=1}^{N}[y_i \log(\hat{y}_i) + (1 - y_i)\log(1 - \hat{y}_i)]$$

- y_i: True label (0 or 1)
- $\hat{y}_i$: Predicted probability from the model

.While test purposes have long been integrated in the design process of semiconductor devices, semiconductor design technology, architectures, verification and testing methodologies are changing more dynamically than ever before. The rapid adoption of AI-based design and verification have opened many scientific challenges and questions across multiple disciplines. Novel algorithms, methods and systems to enhance semiconductor verification and validating of the AI based hardware accelerators are still primarily development and implementation. Deploying new algorithms and architectures in testing must be complemented with new methodologies in verification aimed to enhance test generation and assessment of coverage definitions according to eventual metrics.

The emerging need for planning holistic benchmarks, define oracle metrics and elaborating validation flows aimed to encompass all the newly integrated algorithms and architectures become critical. Old definitions of safety, security and quality require re-explanation and realization. The adoption of and re-examination of these new approaches have significant impact on the design, functionality and power consumption of semiconductor devices. The new design paradigms open novel ways for testing of semantic errors and low-power budgets overall semiconductor architectures. Testability of soon to come algorithms, ways of representing and compressing information will need elaboration as well.

6. Data Acquisition and Management

Novel semiconductor devices will require an ecosystem of measurement tools and software to support their transition from laboratory to the production test floor. Taking memristors as an example, this highlights the necessary measurement steps, from the imaging of a wafer probe yield map through to a device's specification and characterization, before ultimately discussing the creation of an independent programmable measurement and control frontend. A system capable of interfacing to this creation using a PXI platform is included and demonstrates features of software-defined test hardware. Finally, it describes novel device under test control methodologies which ensure the correct interrogation of devices without the need for external proprietary software.

Testing stands as a critical and often neglected step within the development of both novel technologies and integrated circuitry. The ability to be able to interrogate the performance of devices yields valuable information about a device's properties and its design space. This invariably popularizes a device, expediting its move from a laboratory to a production environment. In order for new classes of semiconductor, for example, memristive devices, testing requirements stand as a major hurdle to fielding them [6]. Non-linear, multi-terminal devices with complex internal states pose fundamental questions regarding large icon scale production. This results in multi-faceted challenges, from the programming of wafer probe yield maps to the specification and characterization at device level alone.

Once a test approach, specification, and metric have been classically selected, a testing system must be created. For next-generation devices tested via analog methods the testing environment is a critical step. General-purpose instruments are not designed to be programmatically interfaced to and cannot provide any level of temporal or dynamic control on a device's massive state space interconnectivity. As such, the development of an independently programmable measurement and control frontend is possible. Cardinal for the implementation of systems is their component or architecture selection. Each choice directly defines the potential of a system, from bandwidth through to ease of use. Ideally any systems should be configurable so they can be adapted for future devices. FPGA platforms have become ubiquitous as they offer a highly integrated and performant environment able to

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perform real-time operation yet be re-programmed for future needs.

6.1. Data Collection Methods

The first data collection method is data acquisition from testers and probe cards. These contain measurements from tested chips from the production of semiconductor chips. There are two forms of data collection: direct data extraction from tester machines involving hardware and software reverse engineering, and data pouring from tester machines to production databases [7]. The former can monitor raw waveforms from the test equipment directly, while the latter is usually records of results relevant to test outcomes (pass/fail). The probing timestamps when probing is done on each tested chip are especially valuable, correlating checks on chips with the viewing address matrix of the probe card responsible for them.

In addition to recorded measurements from tested chips (digital array data), residual PC-generated data from simulation are also valuable. These data are commonly split into two forms. The first is related to physical layout, with information on continuity checks, device netlist checks, and connectivity checks presented in the CAD layout view. The second form has to do with SC drivers, test vectors, and parameters. Compact SPICE simulations in node-transistor view are also generated for simulation on low-end machines before production testing, and these contain thousands of SPICE-Script lines of executable MATLAB code. These data also highly correlate with extracts from vectors as inputs to the E8251A testers.

Finally, there are manual interactions from the analysis team to perform failure analysis on bordering die images. The images themselves can also have information encoded into them, such as digitally kernel-processed qualitative and quantitative defect identification. These defects, correlated with failure reasons and physical observations of the silicon die, are documented manually with hash maps, and some of these knowledge can only be deciphered by engineers with experience in the technology.

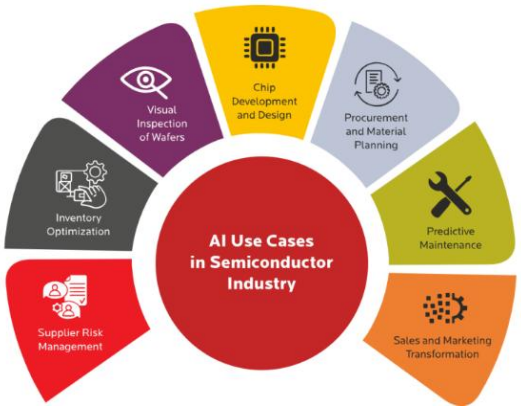

Fig : 3 AI in Semiconductors Industry

6.2. Data Preprocessing Techniques

The authors chose to evaluate the performance of the proposed method based on simulated data sets. Compliance of the independent components extracted by ICA with the theoretical model was characterized with a power spectrum estimate and a correlation matrix. And the performance of the proposed method – detection of devices on which leftover devices could not act on all outputs (missing outputs) – was determined using the same characteristics. In addition, the limitation of the proposed method with devices having a different structure than the mock up process was shown by an example. The proposed method was applicable in the settings of dimensionality reduction techniques based on ICA. Wide and unrestricted signal processing methods could be used after these detections.

Benchmark data consisting of simulated devices based on the distribution of output signal types of simulated devices were constructed for the use of designed methods. Pure signals were assigned to all 128 devices based on two different time stamps used in the mock process. These exported output signals were measured in a noise-free environment using simple and ideal possibilities. Measurement data of devices on flattering distributions were generated in order to mimic a realistic process. Besides output signals on the model devices, Gaussian white noise was added after defining complex noise. The standard deviation was manipulated as an additional parameter, allowing a wider or narrower range of artificial signals. The remaining actions were similar to the previous simulation process enabling the investigation of the behavior of ICA-based technique under a realistic environment.

After data gathering, model fitting, and calculation of divergence, filtering faulty dimensions based on multiple selection strategies would improve output for further

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screening processes. Raw signals with lower dimensions significantly and at once improve visibility, ease operator workload and processing time, and prevent clause exits of unexpected data sources and against strong assumption conditions.

6.3. Data Storage Solutions

Computer systems for deep learning require massive storage, high performance, and high bandwidth. Embedded memories such as SRAM or DRAM tightly coupled to logic elements are a promising solution for on-chip data usage in compliance with these system requirements. However, due to strict timing closure constraints, sophisticated design and retraining approaches are needed to improve NN inference performance while accommodating for imperfections. This paper provides a thorough overview and analysis of FinFET 6T-SRAM-computing-in-memory (CIM) integrated in a 7nm node ASIC platform and equipped with multiple latest in-band weight update capabilities.

Edge applications require fast, energy efficient, and compact storage solutions for continuous data processing [11]. The gap between the power-hungry CPU and storage hierarchy with increasing performance and scaling limitations has inspired hardware-software co-design solutions to mitigate the memory bottleneck. Efforts in proprietary hybrid memory chip architecture and co-design of near data processing systems and software for optimal tensor data movement have been pursued. Excluding advanced neural network architecture-level techniques such as low precision quantization, hardware-friendly architecture exploration and software/hardware co-design for NN inference mapping remains challenging for many systems. ASIC with digital circuit memory components fabricatefully integrated memory processor-in-memory systems with emerging memory devices and hardwired NN function circuits. However, such systems are limited in applications because they need either expensive design iterations or inflexible accelerator architecture, which cannot accommodate emerging hybrid voltage/current mode DNN mapping and off-the-shelf memories with approximated computing and stochastic computing formats.

Possible AI hardware solutions are more or less notable tradeoffs between languages and features. Adopting accelerators as sub-architectures is a more cost-efficient approach. A SRAM-computing-in-memory (CIM) architecture with weight storage in the memory array and binary bitwise computation in the peripheral logic is proposed and compatible with existing backbone technology nodes. A comprehensive overview of design and verification with architecture and domain rank analysis, variable bandwidth, operating margin, and analysis of memory per chip is also provided. Verification IP architecture-tuning, a full multi-way abstraction and layered approach testbench, and a coverage methodology with full functional, structural, and dynamic model coverage to reduce system-on-chip verification effort are also discussed. It enables ASIC VLSI projects to flexibly accomplish advanced hardware implementations with improved verification coverage and efficiency.

7. Testing Methodologies

Testing methodologies can be divided into two sections, namely test methods targeting a specific architecture and test generation methods. Overall, testing can be performed on both the algorithm-architecture and physical-architecture domains. A methodology for testing texture analysis algorithms and architectures has been presented. The ongoing work targets an automatic generation tool. The design introduces a pre-transformed texture in the test method, which is subjected to distinct attacks. A framework for testing dataflow-oriented architectures, which has been used to build a prototype architecture for convolution kernels, has been presented. The tool can generate tests for a wide range of architectures with various organization schemes. Test generation methods in the algorithm-architecture domain can automatically generate tests.

Recent approaches have integrated test generation with core synthesis in order to balance test performance and core efficiency. Efforts have focused on extending the input space to exploit input patterns with fewer cores in the final digit-serial/parallel architecture with less cost/design-area overhead. It has been previously shown that the methodology can be used for iterative algorithms without making any approximation in the test process, and that it can be further extended to find fewer configuration memories with larger dimension by exhaustive searching. Thus, a fully automatic procedure which recursively partitions the core's state space and identifies the appropriate clocks for each subpartition has been developed. Here, the synthesis procedures at both the algorithm-architecture and physical-architecture levels can be a concern, particularly from a production perspective.

Functionally, the core has finite-state machines as inputs and outputs. The behavior of the core has been described in both a functional and a random way. To be able to describe related-to-power behaviors for each of the previously discussed physical architectures, automata-based models have been used. The goal is to synthesize a test probe which, once activated, would generate a specific sequence of states

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for a limited amount of time. Symbolic models of analytic gain, as well as synthesis and partial observation models, have been proposed. Note that the sequential character of the first one can only be modeled with a blackbox representation, while the last one assumes some knowledge of the synthesis objective/architecture.

7.1. Functional Testing

Automated Testing Frameworks 7.1. Functional Testing Testing frameworks for functional testing of next-generation semiconductor devices are discussed. The automatic generation of functional tests for processors, instruction set processors, and systems-on-chip is covered in detail. The evolution of existing methodologies is discussed along with the proper use of synthesizable finite state machines, the specification of architectural state elements, and their state encoding for custom processor testing. Special emphasis has been placed on the testing of address decoders using higher-level functional libraries. The tooling directly generates test vectors for the automatic test equipment platform [12]. The automatic generation of instruction sequences for software-based self-test of processors and systems-on-chip is presented. The proposed approach for generating instruction sequences considers the complete architecture of processors. The instruction sequences are generated based on custom-defined architectural state elements named finite state machines. The design under test is a synthesizable RTL processor. The automation tool takes the architecture, including the synthesizable RTL design and Finite State Machine (FSM) description files corresponding to the architecture, as input. The instruction sequences generated for the FSM and those that can influence the state of the FSM are emphasized.

It can be used to test grey-box and white-box IP cores too. Many approaches have been presented to tackle the problem of functional testing. Earlier methods did not target structural gate level faults. The fault models used were functional. A functional fault model depicts various functionalities of the processor like register decoding and instruction execution. This methodology was enhanced later to include complex instruction execution and cache access. A control fault model was proposed at the instruction level. This method considers the read/write instructions which set up the test separately and has a checking experiment for those instructions. A new methodology for functional testing was proposed. They proposed loading random instruction sequences into the cache and testing the processor using those instructions. This methodology was applied in an industrial setting. It detected many defective chips that passed traditional tests.

Fig : 4 AI in Software Testing – Benefits

7.2. Performance Testing

With continual advances in semiconductor technology, the requirements for next generation devices are becoming increasingly stringent. It is now a great challenge for the device community to meet these requirements and to develop more powerful and sophisticated semiconductor devices. Since the performance testing for high-speed devices becomes more involved and more complex, a testing simulation framework to test and not only validate but to discover these high-speed devices is now needed. As part of this effort, an initial artificial intelligence-based testing framework is presented. Device internal models can be extracted automatically from the incoming device digital test pattern file which is then used in combination with general purpose constraints-check knowledge bases and other constraints to develop efficient test sequencing through satisfiability search solvers. After characterizing the device, this information is fed to knowledge based failure analysis tools to diagnose possible faults/functions/abnormal behaviors causing the failed state. If only part of the response based on the expected from previous characterization is different, artificial intelligence-based heuristic search strategies can be employed to locate the most likely defect/good functions causing the deviation [12].

The performance testing of high-speed devices such as the analog devices in photonics, MEMS and RF, deep sub-micron or fine-pitch devices is confronted with significant challenges. The static, dynamic and internal testing of these devices become very complex and challenging. Automatic testing is thereby very desirable. However, automatic testing for high-speed devices is very challenging. Firstly, the worry is whether more advanced devices necessarily require more advanced and sophisticated testing. Secondly, in the absence of good models, both knowledge based/model based and simulation based automatic testing of such devices is extremely difficult and challenging. Thirdly, secure test strategies are another significant challenge. It is first shown using a mixed problem that under certain circumstances even secure tests can be obtained automatically. Also non-destructive and semi-destructive test strategies are given for safety-critical situations.

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7.3. Reliability Testing

With the dawn of the information age at the end of the 1950s, and with it the invention of information processing devices that transformed items such as pencil/paper-based messages to information processing machines, one can easily recognize how small, discrete systems came together to produce systems that were ever growing bigger. It was when cryptography was first applied to computers that the idea of reliability became paramount in determining the ability of a system to run its code. The term "errors," became synonymous with the term "crashes." As the systems grew bigger and interconnections became too complicated to track, the difficulty understanding became ever more cryptic. The process of tracking the errors became almost impossible.

An insight from the beginning of the quest to make accurate calculations arose when looking at a multi-paper process of simulation, realized that there were 10+ cases in a run and tested the reliability of the system. They predicted the kind of curve below that described the number of papers against time. As soon as a number of papers grew, some divergence occurred, but the underlying cause of these errors was not exposé, being bound up in faith in the nature of computation and devices that were equitable. In just a hundred years, the faith was challenged from several angles of human and machine computation. Two major aspects of their validity were tested here: one as systems grew, reliability became critical and estimates of pursing the pseudo laws of reliability rise carried curve. The second was as research progressed understanding accepted errors came to dominate. The amazing leaps in miniaturization in the last fifty years have more than a century's progress in the same scale of currency. Besides the making of smaller devices, smaller system was also being addressed because of the consonant growth in connectivity and complexity. The philosophy of exploring smaller systems was less effort or cost but clarity in exposition of principles such as searching more ways of displaying the many niches systems have. Very early on, that many detects made non-binary systems had to all operate under a threshold and this alone would mask away understanding simplicity in both the number of threshold and that noise would be independent of size. This seemed an entirety ghost-like path since [13].

8. AI-Driven Automation in Testing

Testing all the components on wafers of semiconductor devices has traditionally focused on checking their functionality. After fabrication, however, defects are sometimes observed that give rise to a reduction in performance or a full breakdown of the active components during normal operation. The test schedule is built from run-to-run, based on the insights from the last test runs, but still results in considerable testing time and resources. Furthermore, new devices with hysteresis effects and nonlinearities are increasingly challenging the automation of tests in the semiconductor industry. Variations of devices from run-to-run are currently considered an obstacle to algorithms using test appearances fed in by the engineers directly. Instead, the testing of each asset is based on low-level electrical signals with model-output diagnosis to increase the follow-up test efficiency.

More effort has been put to develop machine-learning algorithms directly to automate testing for semiconductor digital devices. However, it is still hard to get a broad generalization to tackle the wide variations from wafer to wafer. Two key challenges are stressed. First, the hidden layer distributions across devices may change. In the context of deep learning, this is known as a domain shift. Second, new device designs mean new test configurations for which the existing methodology has to be properly reshaped. To bridge them, graph networks and reinforcement learning were employed for understanding devices' structures, behaviors, and building test schedules. By building a reusable decomposition of the design verification task with graph representation and procedural knowledge learning based on an event-driven simulation engine, flexibility in testing different devices with different technologies can be provided.

The multilayer perceptrons or fully connected networks produce a black-box representation of the correct responses for circuit nets. Using deep learning approaches in testing is expensive and complicated in both model and data. Broad attention is failed to attract in terms of application and settlement. To address this, Hierarchically Spatial and TempOral convolution architecture is studied. It exploits the properties of both the recurrent unit and convolution kernel to replace fully connecting layers and provide further improvement for functional testing of large designs. A sample generation method utilizing combinational logic characteristics can make its applicability and portability very straightforward to individual logic designs. An accurate and fast test generation is covered in detail for large designs with a five-layer variable-sized neural network and a generative adversarial network.

8.1. Automated Test Generation

Automated test generation methods for core-based designs, based on the RTL or gate-level netlists, have been

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surveyed recently. Techniques to perform automated test pattern generation (ATPG) from a structural representation of the circuit are widely used in the industry for testing digital circuits. High-level or behavioral representation of the design, typically expressed in an RTL Hardware Description Language (HDL) like Verilog/SystemVerilog, can also be exploited to derive input test vectors for digital circuits. These high-level test vector generation methods are valuable when the design netlist is not available and in the simulation-based functional validation of a processor and a SOC. With the availability of ATE-compatible test patterns for many industrial design cores, a need arises to validate these core test programs effectively [12].

Conventional simulators cannot test designs that may take several hours or days to exhaustively simulate. Compared to functional simulation, fault simulation is an order of magnitude slower. This is because a conventional simulator needs to execute test patterns, whereas a fault simulator only needs to analyze the state/event result of an executed pattern. Functional test generation is an important, complex, and time-consuming problem. A large number of purely automatic test generators are available today. This is significant because, although there are very accurate simulators for DSPs, the two key problems of test generation for DSPs need to be automatically solved and are still open.

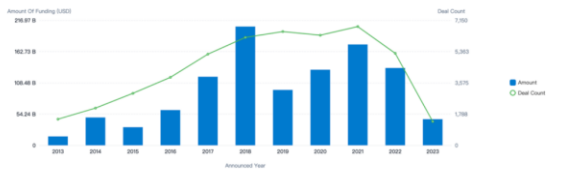

Fig : Artificial Intelligence in Boosting Semiconductor

This paper describes a logic-level test generation system specifically for DSP architectures. The test generation system, provided with a description of the circuit, consists of new test generation algorithms for arbitrary DSP controllers and a set of generic test generation programs for a flexible architecture and a set of DSP specific test generation programs. The test generation programs are based on assignable faults. They can be used both to provide a complete set of gate-level equivalent test patterns and to evaluate a design's testing problems, which is crucial for the design and architecture of DSPs.

8.2. Test Execution Automation

To ensure effective software and hardware integration testing for next-generation semiconductor chips, it is crucial to automate the execution of the defined tests by linking the hardware monitor with the UVM-based testbench. Test execution automation is typically implemented by using the UVM stimulus generation and checking capability in conjunction with standard architecture components. Traditionally, a basic test execution automation implementation is comprised of a three- to five-part component hierarchy consisting of transaction sender, transaction receiver, scoreboard, reference model, and optionally a waveform dump. When using UVM test execution automation, the events in the design under test (DUT), such as message receipts and event occurrences, are monitored. The StartEmmon and StopEmmon commands from the UVM testbench are sent to set up the emmon instance settings after which tests are executed and monitored through the Emmon RX interface with either messages or register reads .

The vis output interface for UVM test execution automation has been communicated from the hardware side by defining a set of messages and a UVM component to encapsulate the monitoring capability; the normal UVM test execution automation components are supplied from the UVM library. Test execution automation implementation based on a special-purpose architecture component, such as a monitor or scoreboard, requires developing new architectural components using the HDL of the design. Such architectural components are harder to modify later and require running a synthesis tool to implement the component on the hardware side. Implementing test execution automation without intervention from the architecture is preferred since it allows reusing or relocating architecture designs with minimal modification on either side.

Existing implementation setups rely on formal protocol documents that will become obsolete with re-implementation of either the testbench or design sides. Introducing a new test will require a test execution automation reimplementation effort due to the different test transaction formats. Implementing an executable version of the protocol in a standardized way that becomes a single point of truth on the configuration and enables easy and dynamic communication between the architecture and UVM would help mitigate difficulties. A protocol description interface or a code generator may assist in producing the message serializer or deserializer on either side. Concerns about test execution automation extend to monitoring the monitoring architecture due to its complexity and performance significance, which warrants custom components to implement monitoring test execution automation.

9. Case Studies

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A framework for robust, AI-enhanced testing of next-generation semiconductor devices, which offer performance improvements over previous generations by providing a multitude of device states, is needed. A key aspect of a chip with thousands of voltage-controlled analysis parameters is bridging the existing test gap between task-based testers that interface with multiple test parameters but have no control over the test settings and task-agnostic testers that present settings exhaustively but test in board-level integrated circuits that are smaller than the chip. In addition, continuous improvements to AI models require flexible frameworks for sensor data collection, structuring, and model training. A novel framework for AI-based testing of next-generation semiconductor devices has been developed, which addresses these needs through novel routines to enhance and reduce the test. It is envisioned that the AI-enhanced structure will change how next-generation semiconductor tests will be executed in the future [12]. A novel testing framework for next-generation semiconductor devices supporting task-based testing developed through collaboration with respective partners. There is an urgent need for testing next-generation semiconductor devices due to their inherent difficulties in generating test parameters despite the improvement performance over their previous generations by offering a myriad of device states. A key aspect of a chip with thousands of voltage-controlled frequency, voltage, and current analysis parameters is the test gap between, on one side, traditional task-based testers that seamlessly interface with a multitude of test parameters but have no control over the specifics of the test settings, and on the other side, task-agnostic testers that present parameter settings exhaustively but test in board-level integrated circuits that are only a fraction of the size of the chip.

A challenge arising from the scan-based architecture of advanced semiconductor devices is in the selection of the start state of the scan test. A novel technique called Local Scan State Setting Technique (L-SST) for a better start scan state selection after these adjustments have been made has been explored. Formalism for the development of models that capture the dynamic behavior of a process design at the device level (in compact form) and the circuit level has been introduced. Testing of software-controlled switched-capacitor single-phase or two-phase sample-and-hold circuits in frequency counting and single-pulse input modes has been considered. Test strategies that accomplish test vector minimization for a compelling class of electronically-testable devices have been presented. On-the-fly test vector generation allows for immediate compact test vector construction as the device information is learned, offering promise for generating compact test vectors. Such test vector generation is particularly needed for ICs being fabricated and probed in a very small prototype quantity.

9.1. AI in ASIC Testing

As device design rules shrink to 5 nm and below, overall chip keeping time is more crucial than ever. As ASIC design teams rush to sign off on their chips, they must deliver the documentation and test vectors used to verify that the chip's design conforms with its specifications. Many ASIC vendors have an internal test group that ensures each manufactured chip is 100% tested. These ASIC vendors are usually fabless companies that do not fabricate their chips. They ship the GDSII design files to a wafer foundry for manufacturing. They also ship the ATE files and documentation used for testing to a different group responsible for testing the chip. All done correctly ensuring each produced wafer is tested for functional, parametric, and maybe even structural defects due to the manufacturing process. However, as the number of devices under test increases in the ATE, the test duration grows, and the amount of vectors to send to the ATE must increase exponentially to ensure proper coverage. Further complicating things, as technology node smaller nodes are being blindly pursued, design engineers are placing multiple blocks on a die containing several millions of gates routed at multiple levels of metal. Most of this effort is directed at decreasing the 3D area or its power but not attention has been placed in ensuring the testability of these gigantic chips [1]. A number of well defined limits exist for the maximizing achievable test time. For one, ATE signal generator speed and bandwidth may be limiting factors. Taking into account skew due to different op-amps, transmission line effects and probe delays, the time needed to drive a net from the ATE on and off may be considerably longer than a simple logic gate delay. Another limit is the propagation delay introduced by combinational logic which can prevent propagation of any faults applied on the primary inputs to the ATE output levels. This delay, crucial design specs and not accounting for temperature, power supply and aging related corner cases all lead to test escapes.

Testing frameworks based on AI for FPGAs were studied. The two major issues in AI-based testing frameworks for SoCs/CPLDs were discussed. One is that a finite-state machine (FSM) or a block diagram is used to model a synchronous circuit. While neural works and deep learning are popular, neither has been adopted for FSM or block diagram. The potential of using a recurrent neural network (RNN) or deep learning for FSMs and fuzzy networks for block diagrams is highlighted. The second issue is that the test delivery needs to execute an individual test. As different kinds of circuits need different types of tests, a possible way of organizing tests based on their types is highlighted [1].

In addition to SoCs and CPLDs, a work on testing FPGA devices is also listed. A loadable finite state machine (FSM)

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for the random test pattern generation of testing embedded DSPs in FPGAs is introduced. The key issue is to find a checkable fault model for temporal fault behavior. A few simple test patterns are given as an example to show this algorithm. The example is tested on the organizational chart of the Xilinx FPGA embedded DSP architect without considering the area of the circuit. A new test pattern generation algorithm for temporal cycle slip fault tests of TPG-based built-in self-testing of FPGAs is proposed. The calculable f-mode as well as a highly simultaneous and effective compact test pattern generation algorithm for TPG-based BIST is also introduced.

Eqn : 3. Signal Integrity Model (RC Delay Approximation)

$$t_{delay} = R \cdot C$$

- t_{delay}: Propagation delay
- R: Resistance
- C: Capacitance

Used to evaluate timing characteristics during test.

A loadable FSM for the random test pattern generation of testing embedded DSPs in FPGAs is also presented. The proposed TPG is based on a geometric multi-valued random algorithm to reduce the MTTF. With the proposed loadable FSM, the proposed TPG can be used for the built-in self-test of the sequential unit of a modern DSP in an FPGA. The encrypted test patterns can be loaded into a loadable FSM on hardware during production testing. Once loaded, the transparency of the TPG operation is hard to breach, especially for the random generation TPG.

Data choices evident while building the distributions: Validation SCs: 80% of SCs. Training: 10% of SCs. Testing: 10% of SCs. Response predictions: Realistic. Peak power density provided using a distribution for variability. PCT query retrieves parameters for SCs to create and query speed simulations. Simulation sequences: 2s, 150s, and 1ns per SC per tested chip. Injection profile: Simulated injection tests over 9 workloads, screen time 48s. Combined profiles simulated for over 4 days over those workloads. Each chip's different loaded efficiency and number of SCs prune potential injections from first testing. Variability rally identifies realityindicating SCs and generates ICs. One IC and actionable heavy task can account for 10-20% of peak power prediction error. Symmetric messages cut down workload and timing pools and increase rally speed. Batch-wise races combine several chips and ranked setups to reduce rally time.

Overall, the presented case study demonstrates the value of a framework integrating fast-ahead AI and distributions for SCM diagnosis, in terms of elevated decisionmaking accuracy, coverage, and speed. Nevertheless, bias in training data must be addressed to better generalize to applications out of distribution. Moreover, to boost production diagnosis, model validation completeness becomes important, which is especially challenging when resource-driven sampling must be attempted, presenting opportunities for further research. Intelligent AI-based Scheduling for Parallel Production Test in 2.5D ICs. Algorithmic nature amongst structures and access difficulties with state information make automatic scheduling across diverse parallel ICD blur in theory, and in practice, estimation and its evaluation in 2.5D heterogeneous systems are costly and slow under state complexity growth. Online distance-ratio greedy method generates good test assignments in terms of adaptability and speed for Routing Planning of 2.5D Test. Combined with runtime analyses on Evaluation-Consistent Tests, this framework can be well-applied and evaluated for general ICD as balanced condition becomes more practical than rigorous state equivalence. In the cases examined, the speedup is desirable and the assignment quality holds.

10. Evaluation Metrics for Testing Frameworks

Evaluation is an essential and challenging part of testing frameworks and has been specified as a key aspect to be considered in evaluating testing frameworks. Evaluation aims to assess the testing framework, the capability of the testing framework with respect to various test goals, and the generated test cases with respect to various evaluation metrics. A plethora of evaluation metrics exist to evaluate the general testing framework. Besides that, forming a foundation of evaluation metrics tailored to black-box AI-based testing frameworks is equally essential due to both the properties of AI-based systems and the existing black-box testing frameworks. Menacingly failures of autonomous systems could result in loss of life, property, or reputation. Thorough testing is essential to present convincing evidence of system safety before deployment.

To this end, generative black-box testing frameworks that can generate tests and validate the output of complex autonomous systems are essential but challenging to develop. Very few testing frameworks exist and address only a subset of the required properties while relying on the non-trivial setup of white-box components. In addition, such frameworks can only be used by testing experts to capture the completeness of the generated tests. Therefore, a general fully black-box testing framework that can generate tests for

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autonomous video object detection systems at runtime while being easy to setup and use is sought. To this end, formally define the properties that make up such a general testing framework by building upon the existing evaluation metrics for AI-based testing frameworks.

The black-box testing framework is within reach, and prototyping pipelines for runtime test generation and evaluation of such systems is also vital. A case study of an intelligent traffic management system is conducted to provide a concrete demonstration of the black-box testing framework. An extensive set of testing goals, test properties, and evaluation metrics is outlined with respect to the black-box capability of the testing framework. The concrete choice of properties covered by the prototype is also justified. An introduction to how to setup and use the prototype and some real-life testing results that demonstrate the performance of the prototype are presented. Testing is a popular and widely-used technique for ensuring the reliability of software systems. In recent years, AI-based approaches have been proposed and widely adopted in many areas such as computer vision, natural language processing, and game playing.

10.1. Accuracy Metrics Next-generation AI-based accelerators consist of densely placed heterogeneous processing elements (PEs). A PE can comprise multiply-accumulate (MAC) units, digital logic circuits, memory arrays, or weight storage. Because these PEs perform arithmetic operations on a large number of inputs through tight schedules, they are more susceptible to failures, particularly systematic defects caused by manufacturing variations. Although safety nets can be added, this causes significant overhead in area, power, and performance. With a high degree of process variance, the increase in systematic defects could lead to excessive yield loss and delays in time-to-market. Recent AI-based accelerators consist of 30-100 billion transistors and inquiries to hundreds of thousands of PEs. However, even state-of-the-art test resources with a large test throughput are likely to test only 5-15% of PEs in the time available for manufacturing test.

Other accelerators like GPUs and TPUs continue to scale horizontally by packing more transistors and adding up to thousands of PEs. Being packed in a small chip footprint, circuit faults in these PEs could significantly degrade performance. At the same time, more chip resources for auxiliary circuitry to recover yield could drive the cost up by tens of millions. Because of the tradeoff between success-failure/speed/cost, accuracy-resilience offers an avenue for yield recovery through design-level approaches without hardware modifications. AI tasks are largely irreversible; the stochasticity of backprop-based training can provide bounded error resilience, even in the presence of faults. So, it is speculated that as many weights, PEs, and synapses are disabled, the result of widely used DNN tasks could remain within acceptable bounds. Using software techniques for drop-out, pruning, and quantization of weights, the area and power of the designs can be severely reduced, and acceleration, lessening memory power consumption, can also bring an accuracy-tolerance dimension to the design space.

10.2. Efficiency Metrics

For characterizing the performance of a testing framework, different metrics can be utilized. Throughput relates to the number of units tested per time unit and is dependent on the test configuration. For a given test set containing m tests for a design with k test configurations, with Tj being the time it takes to apply a test j, where $1 \leq j \leq m$, the throughput is derived from the following.Throughput = Number of units tested / Time

It can be seen that throughput is dependent on test application time, number of test configurations, and number of test sets. In characterizing testing framework performance, throughput cannot be directly employed as it depends on many factors. Therefore it is often abstracted and that depends only on hardware design but not on the test set composition is desired to evaluate testing frameworks. Two metrics are proposed as follows.

(1) Efficiency of Configuration: Given M configurations and N tests (or lumped tests), efficiency of the configuration is defined as the time unit resource used by a unit test.

Efficiency of Configuration = Max(T1, T2, ..., TM) / (T1 + T2 + ... + TM)

Where Ti is the total test application time of the ith configuration. To be a unit test, a configuration should be selected from those that take less time than all others in accordance with the current test set in application. The efficiency of the configuration in a failed configuration can be regarded as a ratio of time unit resource consumed by the configuration for the corresponding test set to the maximum test application time of all configurations.

(2) Efficiency of Design: Given N tests, D designs, and M configurations in each design, the efficiency of the design

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with respect to the time unit resource consumed by the corresponding testing framework is defined as the maximal resource enhanced by re-distributing tests on the current test set among different designs, whereas a design beyond the available configuration cannot be used in the evaluation.

Efficiency of Design = (Max(0, Efficiency1, Efficiency2, ... EfficiencyD) + 1) / 2

10.3. Cost Metrics

Cost metrics, or factors that cost f's, often behave like accuracy metrics, or factors that measure how good some criteria are. The only difference is that relatively few desirable criteria (parameters) are subjected to cost metrics, though an exhaustive list of cost metrics for event-test-model simulation systems can easily be lengthy. Potentialities of interest include tester cost, test program, test execution time, and macrospatial size. Cost metric expressions are either numerical parameters themselves or functions of numerical parameters that map into numerical parameters.

Cost metrics can be either unrestricted or restricted. Unrestricted cost metrics take on real-number values that are unbounded and unrestricted. Restricted cost metrics are computed from uniformity over some set of numerical domains, and the worst-case cost metric for the configuration is translated into a unique (uniform) value in some metanumerical domain that conveys more information than the numerical values of its constituents do. The value in the meta-numerical domain is then derived from the direct computation of the worst-case cost metric on the constituents' numerical domains [14].

Potentialities of interest are either ordinal based and given language lexical interpretations or cardinal based and strictly numerical so that at least a portion of their numerical domains is composed of integers only. However, the strength of cardinality or the rigour of the interpretation given to the potentialities is not of direct concern. Potentialities should either, by numerical computations, yield some unbounded numerical values, or uniformly by some worst-case meta-numerical value.

11. Integration of AI Frameworks into Existing Systems

Integration of AI Frameworks into Existing Systems.The fast-paced advances in the semiconductor industry are creating further challenges for AI-based testing frameworks. Since the deployment of AI-based semiconductor devices is just at the beginning stages, working on a generic AI-based testing framework that can be integrated into existing verification testing flow is a huge challenge. Another challenge is that many of the AI-based designs target one specific application area for automotive, big data, or cloud, and they do not pose a great need for a generic solution that can cover a wider application area. In addition, converting RTL to netlist and post-layout parasitics is becoming an essential part of the verification process. Fast adaptation of AI-based testing frameworks in the existing testing flow is difficult to achieve.

Addressing all the aforementioned challenges is necessary to build a robust AI-based testing framework that can keep pace with the fast-growing semiconductor industry. Considering the fast advancement in the semiconductor industry, starting with the better form of design representation data, metadata of the circuits relating to edge-case design criteria, etc., is considered as the scope of the research. Developing an automated testing framework for custom test pattern generation and full-chip testing of telecom chipsets has been a significant development. A terabit search engine ASIC, a 33M-gate chip containing custom designs, a 14-ns, 48M-bit SDRAM, and protocol testing chips were manufactured and tested using this framework. Similar frameworks have also been developed in other disciplines. In a field programmable gate array manufacturing, a low-cost production test system providing fully programmable on-chip test capability, custom on-chip instrumentation, and scan-based, built-in self-test architectures has been developed.

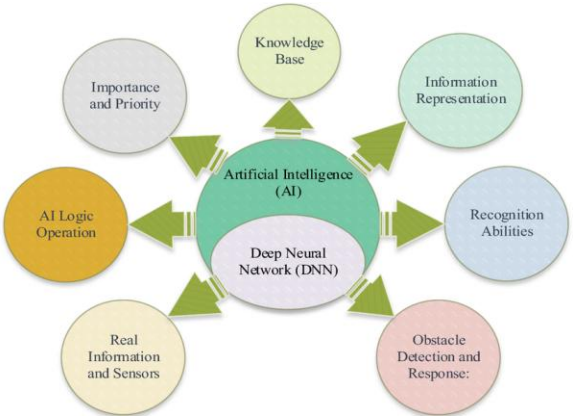

Fig : 5 Artificial intelligence framework

Developing a practical AI-based testing framework is not just assigning AI tools in the verification flow, creating more automation, or generating comprehensive tests from all design corners. Creating a good AI-based testing framework needs to understand the intricate balance among pervasiveness of the application and its architecture, workload adaptation vs algorithmic precision, input-aware

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analog computation and architecture saturation, power supply and clock/gating. Integrating cutting edge AI hardware designs requires developing new testing innovations as well. Most importantly, there is no off-the-shelf testing framework that can directly adopt these designs. Studying edge-case design criteria from silicon data itself should be the key for future testing research focus.

12. Future Trends in Semiconductor Testing

The evolution of semiconductor VLSI testing technologies has also affected digital and mixed signal domain ICs. On the mixed-signal domain IC testing front, following the apparent successes of alternate and RF technology in the market, new trends on testing and reliability front are evolving. With the rise of 5G devices, such systems' complexity will rise, leading to a further need for advanced knowledge on the performance of the devices involved. However, while this reliability has gained increased attention over the last decade, it is becoming clear that there are challenges ahead. A way to quantify reliability is reliability physics, but these methodologies and models are not automatically suitable and need adaptation for various fields. As a still relatively new field, the integration and availability of multi-domain information representation models and notation standards is sparse and actively the object of early development. Another issue is the increased complexity of systems, which makes it cumbersome to identify reliability-critical states, transitions, and failure modes [1]. On the other hand, Semiconductor-IC testing has evolved across the various domains and ever-increasing levels of complexity. To address the testing of increasingly complicated devices Artificial Intelligence-based tools/workflows have become more generic, making use of ML algorithms more focused. Many of these "futuristic" solutions will impact design opportunities as well as performance themselves and thus usher in entirely new testing methodologies. AI-driven test synthesis solutions have shown improved test quality and reduced test cost in many scenarios. More importantly, these tools address large and complicated scenarios across various design paradigms, which would be nearly impossible to implement or evaluate manually.

12.1. Emerging AI Technologies

Threnshо Institute of Technology has studied longer than a decade the innate high ambient energy efficiency of analogue computation based on devices with physical nonlinearity. Semiconductor devices based on fluid dynamics with low frequency oscillation and ultrafast response times have been used to implement two-dimensional (2D) reservoir computing a rich class of learning networks based on complex spatiotemporal dynamics in real-valued 2D delay feedback systems. Research on devices based on coupled oscillators are gaining momentum to chart novel learning paradigms, such as those involving spiking neurons and analogue synapses. The adaptability of devices in terms of learning time and available parameter space to explore is a major systematic challenge, considering the speed, variability, and parasitics of quantum dot laser DMLs along with the stringent fabrication requirements and costs. For the responsive time of 250 ps, a learning time of 20 ms can be achieved, while the degree of symmetry of lasers used varied substantially. Analogous to the natural selection of traversed DML parameters, this results in the discovery of a 95% test accuracy that rivals DMLs with the same topology and hyperparameters. Several spectra of gain and delay responses exhibit the system's memory retainment, with multi-peak gaining the largest memory efficiency.

Software simulation is often provided to explore the software framework and devices deep learning tasks via spiking neural network languages and neural architecture search methods. However, GDML devices have their own shortcomings in deep learning such as explicit training costs per image of inferences and inflation hardware deployment footprints to accommodate weights storage. A progressive structure and layout method is then proposed to achieve resilient on-chip learning inference to handle GI. Moreover, significant progress is presented on utilizing conductive nanostructures in volcanicenergy training sDMLs more applicable to real-world AI tasks, especially for near-sensor and on-chip learning scenarios. On the other hand, learners trained under a network truncation are found to maintain consistent inferences across diverse deployments.

12.2. Trends in Semiconductor Design

Semiconductor devices are placed inside systems such as well-defined functions. In functional terms, they usually become block diagrams. System-level testing is executed using behaviors of such block diagrams in a purposeful manner. Automated testing is done through a test-bus and a compacting vector tree structure using a standard protocol to minimize routing complexity in order to computer test time for high throughput. Test time is compared with algorithm implemented test time at the device design time to ensure that a detector design change is functional. Chip-level testing takes place at wafer test before trimming where high-speed functional testing techniques

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based on burst-sampling are implemented. AI techniques are utilized to seek out bad chips to minimize probe time durations. The reliability of semiconductor devices becomes a major issue when they are incorporated into larger systems, because system-level DUTs are often out of the realm of detection by means of voltage and current measurements. With TE vibration and crushing effect, burned-out fails are presented that cannot be detected at a system level. To catch them at a device level as soon as possible, reliability test structures are constructed that can be used for c-bin inspection afterward. Using the same structure, reliability tests of devices undergoing challenge tests can also be performed before their packaging.

AI techniques are extensively applied for in-depth inspection of the reliability test after stress as transient ringing on MOSFET turn-off high-side driver patterns holds information on bad devices. Knowledge-based diagnosis tools successfully classify randomness in terms of their waveforms, which correspond to multiple failed devices on a die. The proposed waveforms are also analyzed based on detection sensitivity by calculation of thumbprint waveforms. For smaller and faster devices with higher complexity, robust design is needed. A voltage step changed examination technique after hot-switching feet successfully catches out-of-spec devices. A MEM DMD and gate-speed gradual-change control are developed for lower versions of devices subsequently released in order to avoid burn failures during probing. AI techniques are utilized to extend manufacturing capability by busy-unit utilization predictive modeling. For devices having rare fails, rather than detecting suspect time stamps, aid text mining techniques are utilized to predict defective machines. Detection units that can be used as the floor plan of scores are developed so that the risk of undetected fails can be reported. The above techniques are well-validated in high volume testing of mass-produced devices.

13. Ethical Considerations in AI Testing

The past decade has seen an extraordinary rush in the developments of Artificial Intelligence (AI) technology and applications. The wide-ranging adoption of AI for various applications, such as health care, finance, and employment, among others, has resulted in concerns regarding the reliability of AI models for these critical applications . In order to curb these concerns on the reliability of AI models, AI model testing has become a key area of research. Intensive research efforts have, thus, been directed toward testing classical models like software and machine learning based classifiers, and various testing techniques testing frameworks have been put forward. Various tools for testing of classical models like software defects and fault-based testing have been proposed. Most recently, testing of spam filters has been suggested. Similarly, testing techniques and frameworks for the testing of ML models has been actively researched in the recent past. Some feature perturbation based testing techniques for testing of ML models have been suggested, along with a framework called TESS for testing ML classifiers that utilizes fuzz with input perturbations to generate adversarial inputs. A series of attack-based testing frameworks for testing adversary removal techniques of ML models have also been proposed. On similar lines, testing techniques for the metamorphic properties of fairness, and robustness of ML classifiers have been put forward. As key governance aspects, ethical considerations in testing AI/ML models with the aim of fostering trust and confidence is an active area of research. In this context, this article discusses key challenges for testing ethical properties of AI/ML models and suggests potential solutions to address these challenges. Ethics in AI has widely become a topic of discussion within the industry, academia, and regulatory bunker. The ultimate expectation from AI is to improve productivity, work satisfaction, and efficiencies in the society and organization [16]. There are many ethical consequences and challenges for AI based systems as the growth of AI/ML/Automation is expected to be more ubiquitous. These ethical challenges mainly arise in two parts namely, ethical aspects during design time and testing time of AI models. Ethical design principles such as fairness, transparency, accountability, and security are actively researched areas. Apart from design principles, monitoring of ethical properties of AI models during testing phase is equally important.

14. Regulatory Standards and Compliance

Regulatory standards and compliance are critical components of safety during the design, fabrication and process of any type of semiconductor devices. Semiconductor device design requires compliance to for another reason; design, fabrication and implementation are immensely different processes. Architecture and design is done on a high level. Libraries and tools that are used during design can't be used after they have left the CAD domain. Therefore, additional attention is paid to surveillance of the foundry by regulatory agencies and/or standard giving bodies [7]. All of which have their strict compliance regulations. Additionally, some devices remain classified due to national security concerns. Simple devices are usually done in-house on mature or proprietary technology at a trusted foundry. The advantage is that process weaknesses or non-compliance is easier to fix. More advanced devices, usually MEMS based, require scanning of process

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technologies on a weekly basis. In this case one or more fabrication processes to which the design has to comply are selected by an implemented interface. This can include fixing crooked mirrors, adding an additional oxide layer, changing a thickness or not allowing via cuts in specific layers. Stage-Gate procedures and vendor design rules much like IEEE Std 1500 go one step further to assure both foundry compliance and device robustness.

Much effort is spent on design-for-assembly and design-for-manufacturability aspects. These aspects are very different from that of IC's. General procedures and rules are by all foundries and there are some commercial tools. But these tools are mainly utilized by the fabricator. To speed up the process and improve robustness of the designs, both in-house and COTS tools are utilized. Additionally, the through silicon via designs of MEMS and stacked ASIC's were integrated and rules were developed .

15. Conclusion

With the fast development of AI techniques in design and manufacturing, a pressing need of the semiconductor industry is to explore the feasibility of harnessing AI capabilities for the verification and testing of new-generation devices. Some application opportunities in the design and manufacturing stages of semiconductor devices and the revisions of established standards are identified. Early engagements and investigations are discussed in regards to AI-Aided Test Engineering Frameworks (AI-TEF) that can support further exploration. The initial version of some sector and domain applications and AI-ML aware extensions of related design and manufacturing tool chains are presented. It is predicted that by 2030, AI would yield significant contribution to semiconductor verification and testing among other domains, and establish a high-level industry standard of best practices. Addressing both the urgencies and importance, opportunities and challenges of harnessing AI capabilities for semiconductor verification and testing are discussed .

It is predicted that by 2030, AI would yield significant contribution to semiconductor verification and testing among other domains, and establish a high-level industry standard of best practices. Since 4 years ago, substantial fast achievements on discovery of advanced AI methods, adaptive exploring the design and manufacturing circuits have been addressing design challenges of verification and testing. At the same time, this has also raised challenges for establishing new standards to harness AI capabilities. For testing and/or testability, the revision of the effectiveness indicators and the penalties to AI-aided information flow obfuscation could be easy milestones to reach. More comprehensively, establishment of acceptability indicators and rules, which can be evaluated as rigorous as 5 sigma with blind test, would be a tough challenge cross multiple technical domains.

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