

Energy-Efficient Clocked Storage Elements for Low-Power VLSI Systems Using Conditional Capture Mechanism

A.Udhayakumar^{1*}, Nivethitha T², Arunkumar Munimathan³

^{1*}Department of Electronics and Communication Engineering, VSB college of Engineering Technical Campus. Coimbatore, Tamil Nadu, India. udhaya2k6@gmail.com

²Department of Electronics and Communication Engineering Sri Eshwar College of Engineering, Coimbatore, Tamil Nadu, India nivethitha1704@gmail.com

³Department of Mechatronics Engineering, Hindusthan College of Engineering and Technology, Coimbatore-641032. mraranapdpi@gmail.com

Corresponding Author: udhaya2k6@gmail.com

Abstract

The growing need of energy efficiency in the Very Large Scale Integration (VLSI) systems used in portable and high performance computing devices requires designing low power sequential elements. Flip-flops and latches are clocked storage components, which are major contributors of total power consumption because of intense clock switching. The present paper is a proposal of an energy-efficient clocked storage architecture where a conditional capture mechanism is proposed to reduce unnecessary switching, which is minimized by conditional enabling a data capture only when input transitions are made. The design proposed is a combination of clock gating and data-dependent control logic that has minimized dynamic power dissipation and still enabled the design to operate at high speed. The architecture is analyzed with CMOS technology at 45 nm and 28 nm node with simulation in Cadence Virtuoso. The performance measures such as power consumption, delay, power-delay product (PDP), and energy efficiency are examined and contrasted to the traditional master-slave flip-flops and pulse-triggered flip-flops. The results illustrate a large decrease in clock power and switching activity, and the introduction of up to 35-50% power savings without a high degree of propagation delay effects. The designed product is suitable in low power applications like IoT gadgets, wearable electronics, and embedded systems.

Keywords: Low-power VLSI, conditional capture, clock gating, flip-flop design, energy efficiency, dynamic power reduction, sequential circuits.

1. Introduction

The blistering development of portable electronics, Internet of Things (IoT) systems, and high-performance computing systems have made the need to design energy-efficient Very Large Scale Integration (VLSI) circuits much higher. The digital systems that are currently modern are supposed to provide high levels of performance in terms of computations and work under strict power limitations especially in battery powered and energy sensitive systems. It is against this background that optimization of power consumption at the circuit level has become a design priority. Clocked storage elements, including flip-flops and latches, are some of the other building blocks of digital integrated circuits, and they are central to the determination of system performance and energy efficiency. They have extensive applications in pipelines, registers, and memory interfaces and when frequently switched, these sequential components significantly add to the overall power dissipation. The clock distribution networks (as well as other sequential elements) have been well-known to contribute to about 30-50 % of the overall chip power dissipation in synchronous systems. This is because power consumption is more than normal as a result of the constant switching of the clock signal which results in a high capacitive load over the circuit. CMOS technology is characterized by switching activity, load capacitance, supply voltage and operating frequency as controlling dynamic power dissipation. With the increase in the scale of technology and decrease in clock frequencies, the effects of switching activity is even greater. The traditional flip-flop schemes, including master-slave ones, are used by activating internal nodes at each clock edge, irrespective of the change of the input data. This causes unnecessary charging and discharging of internal capacitances hence unnecessary energy consumption. Redundant switching inefficiency is enhanced in large-scale synchronous systems, where large fan-out clock signals are distributed over large networks. Within this type of systems, a minor decrease in switching activity can result in big power saving in the chip level. In order to overcome these issues, a number of low-power design methods have been available in the literature such as clock gating, pulse-triggered flip-flops and dual-edge triggered flip-flops. The idea behind clock gating methods is to apply zero or some delay to the clock signal when it is not necessary to conduct any useful computation, minimizing dynamic power. Pulse triggered so-called flip-flop designs minimize the count of clocked transistors, a single latch structure is used, and dual-edge triggered designs record information on both clock edges to reduce the actual frequency of the clock. Although these developments have been made, current solutions tend to trade-off the power consumption, propagation delay, circuit complexity and robustness. Specifically, not all designs eliminate entirely redundant internal switching which is an important source of energy loss. Also, some low-power techniques may have a complex control logic, which may also result in higher area overhead and worse timing behavior, making their use in a high-speed system restricted. To address these constraints, this paper will present a new architecture of Conditional Capture Flip-Flop (CCFF) which will make use of a data-dependent switching mechanism in an effort to avoid unnecessary internal transitions. In the proposed design, there will be a transition detection logic at the input to be able to capture data only when a significant change is detected. Incorporating this conditional capture mechanism together with a technique of using an efficient clock gating strategy, the design has large switching activity and dynamic power consumption. In contrast to the traditional methods, the suggested one will help to maintain internal nodes in a stationary state in idle conditions, which is why the unnecessary transitions will be eliminated without causing a significant load on the delay. The work has a complex contribution. The suggested CCFF proposes a new architecture of low-power sequential design, which is capable of balancing energy consumption and performance. An analytical model in detail is created to measure power savings made in terms of reduced switching activity. Implementation and validation of the design is done using state-of-the-art CMOS technology nodes, which makes it relevant in practice. Additionally an extensive comparative analysis is carried out against traditional flip-flop architectures to establish the excellence of the proposed architecture in regard with power consumption, delay and energy efficiency. In this work, a solution that is scalable and robust is provided to next-generation low-power VLSI systems.

2. Related Work: Clocked storage element low-power design is an area of active research, mainly due to the sequential circuits being the largest portion of the total power consumption of integrated circuits [1,2]. The master slave flip-flops (MSFFs) remain pervasive due to their strength and simplicity, however, it requires a lot of dynamic power to operate due to the constant clock switching and unnecessary state transitions in the internal nodes [3]. This has led to the widespread research on clock-gating techniques to reduce the extraneous switching by turning off the clock signal in the absence of data transitions, thus reducing unnecessary activity [4]. Despite this, clock gating not only adds control circuitry which may cause clock skew but can also increase timing complexity especially when used on large systems [5]. Pulse-driven flip-flops (P-FFs) can be introduced as a new technology, which replaces the two-stage master-slave design with a single latch with a short pulse of the clock [6-8]. Subtractions in transistor counts and clock loading are then realized, although P-FFs tend to have difficulties with pulse -width control and increased short-circuit energy on high-frequency operation [9-10]. Another interesting category is the dual-edge triggered flip flop (DETF) which records both rising and falling clock edges; the bidirectional sampling allows the clock frequency to be lowered without

reducing throughput and hence dynamic power can be reduced [11]. But DETFF designs usually involve more complexity of the circuit and higher leakage currents. Other suggestions include conditional capturing and conditional precharging methods that seek to do away with the unnecessary switching by detecting input activity and only allowing internal transitions when needed [12-15]. The switching activity is significantly reduced with conditional precharge flip-flops (CPFFs) but additional latency is possible because of the evaluation logic necessary. Recent developments focus on information sensitive and adaptive flip-flops where internal nodes are biased in switching to suit current conditions of inputs. Such strategies offer significant power savings, but often they involve trade-offs as far as area overhead is concerned and architectural complexity [16]. This notwithstanding, achieving a perfect balance between the power, delay, and robustness remains a daunting task. The paradigms of contemporary designs tend to sacrifice speed for power or use complex control logic which affects scalability [17-18]. Within this context, the given conditional capture mechanism aims to provide a moderate solution, which will reduce unnecessary switching, maintain high-frequency operation, and reduce the complexity of design [19-20].

3. Proposed Conditional Capture-Based Flip-Flop Design

3.1 Design Overview

The suggested Conditional Capture Flip-Flop (CCFF) implements a data-dependent switching logic to minimize extraneous internal transitions of sequential circuits. Under the traditional flip-flops, the clock signals cause the internal nodes to swing irrespective of input data variation and the extra switching activity and high dynamic power use results. This limitation is defeated by the CCFF, which includes a transition-aware control logic, which only triggers the storage mechanism when there is a meaningful change in the input in Fig 1. This selective activation has a great impact in minimizing switching activity, therefore the design is very much appropriate in low-power VLSI applications.

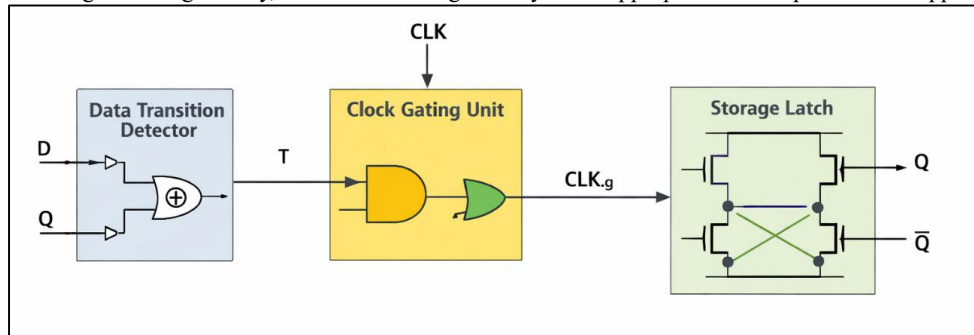


Figure 1: Proposed Conditional Capture Flip-Flop Architecture

3.2 Transition Detection Mechanism: The main principle of the suggested design is the transition detection mechanism that compares the current input D with the previous output Q that is stored in the memory. The implementation of this comparison is carried out by use of XOR logic function that produces a transition signal that is as follows:

$$T = D \oplus Q$$

$T=1$ implies that there is a change in input and some capture operation would need to be done. On the other hand, at $T=0$, no transition is observed and the flip flop is left in an idle condition. This is done by this mechanism such that switching activity is only possible when needed, which practically minimizes unnecessary power dissipation.

3.3 Conditional Clock Gating Strategy

To extend the power efficiency, a conditional clock gating circuit is controlled with the help of the transition signal. The signal of the gated clock is presented as:

$$CLK_g = CLK \cdot T$$

This will make sure that the clock is only propagated to the internal nodes in the case of active transitions. In the event no change in input is observed the clock signal is suppressed and this avoids unnecessary switching of internal capacitances. This does not only minimize dynamic power, but short-circuit currents due to the frequent switching are also minimized.

3.4 Circuit Operation

The work of the CCFF can be perceived in roles of active and inactive. When D is not equal to Q in the active mode, the transition detector enables the gated clock so that the new information can be stored at the storage node. However, in the idle state, when $D=Q$, the gated clock is disabled and the internal nodes are left in their last state with no switching taking place. This two-form functionality is sufficient to provide a high level of power usage, at the same time, preserving proper logical work. Transistor level care is taken to be sure that the extra logic is not a major delay. This way, the high-speed performance of Fig.2 is maintained.

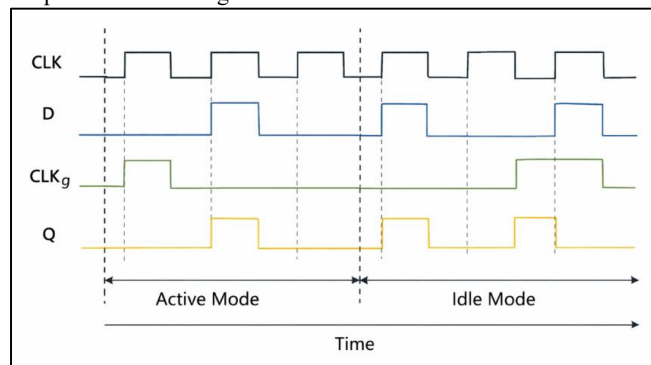


Figure 2: Timing Waveform of CCFF Operation

4. Mathematical Power Modeling

4.1 Dynamic Power in Conventional Flip-Flops: Dynamic power consumption is the most important element of total power dissipation in CMOS digital circuits, especially in high-frequency synchronous systems. The sources of this power are mostly related to the repetitive charging and discharging of capacitive loads at loading nodes and output nodes as part of switching events. Mathematically, the dynamic power consumption is as:

$$P_{dynamic} = \alpha CLV^2_{df}$$

Traditional flip-flop designs have the switching activity strongly dependent on the signal (clock) which periodically switches on or off depending on the clock cycle, independent of whether the input data transmits new data. This causes charging and discharging of internal capacitance many times even when idle condition occurs and no useful data change takes place. Thereby, the switching activity is effectively high resulting in high dynamic power dissipation. Moreover, the existence of repeat transitions on internal nodes is also an added contribution to more energy wastage. This inefficiency is further exacerbated in large scale VLSI systems in which large number of flip-flops are driven by a global clock net.

4.2 Switching Activity Reduction in CCFF: The proposed Conditional Capture Flip-Flop (CCFF) is a solution to all those inefficiencies of the traditional designs, as it introduces a data-dependent switching model which minimizes superfluous transitions. Under this scheme the effective switching activity is no longer defined by the clock signal only but rather by the likelihood of transitions of input data. The altered switching activity may be stated as:

$$a_{\text{eff}} = a_{\text{clk}} \cdot P(D \neq Q)$$

where $P(D \neq Q)$ is the transition probability of input data. This is a significant reduction to the overall power usage since the vast majority of practical digital systems have small transition probabilities. In real-life digital systems, the input data is frequently correlated in time akin to the case of the video game, so the transition probabilities are usually still very low. Using this property, the CCFF has a strong capability of minimizing the effective switching activity, which reduces the dynamic power consumption. In addition to this, unnecessary transitions will also be suppressed thus reducing internal node toggling which again leads to a saving of energy. It is a data-conscious switching framework, a radical break with traditional clock-based designs, and an input-based operation, which allows more effective use of power.

4.3 Power Consumption of Proposed Design: The proposed CCFF can be modeled to have a dynamic power consumption by implementing the lowered switching activity as well as the impact of conditional clock gating. The expression of the power of the CCFF is as follows:

$$P_{\text{CCFF}} = a_{\text{eff}} C_{\text{eff}} V_{\text{dd}}^2$$

The effective capacitance of C_{eff} obtained following clock gating. The effect of decreasing the switching activity and effective capacitance to reduce the power dissipation is an addition. The net effect of this twofold reduction in switching activity as well as effective capacitance is significant dynamic power consumption reduction. Also, conditional capture mechanism will lower the short-circuit power by minimizing parallel conduction paths at switching. It also inhibits transitions caused by glitches which are usually the cause of further power loss in high-speed circuits. Consequently, the proposed CCFF has better energy efficiency without necessarily demanding tremendous alterations in the circuit structure.

4.4 Power Saving Analysis: In order to measure the goodness of the proposed design, the saving of power by the CCFF is considered to that of traditional flip-flop design. The percent of power conservation can be woven as:

$$\eta = \frac{P_{\text{conv}} - P_{\text{CCFF}}}{P_{\text{conv}}} \times 100$$

This is illustrated by the wording that the effectiveness of the CCFF is high when the probability of transition of the input is low. Also, low switching activity also minimizes short-circuit power and glitch induced transitions further leading to energy efficiency. The above expression shows categorically that the power saving is highly contingent on the decrease in switching activity. The effective switching activity is lower as the probability of input transitions is less, resulting into a greater energy saving. This is especially beneficial to the CCFF when the data activity in a given application is low, like in control circuits and memory elements. Moreover, the decrease in switching activity also leads to the reduced short-circuit currents and decreasing glitch propagation, which increases the power efficiency and signal integrity. All these enhancements combine to achieve a solid and scalable solution to low-power VLSI design, which makes the proposed CCFF very appropriate in next-generation systems with energy-efficient systems.

5. Simulation Setup and Methodology

5.1 Technology and Simulation Environment: The proposed Conditional Capture Flip-Flop (CCFF) is modeled and analysed via a transistor-based simulation framework within the Cadence Virtuoso environment and offers a sound platform to perform a precise circuit level analysis. This implementation is undertaken with 45 nm and 28 nm CMOS nodes of technology to represent developed and advanced semiconductor technology. The modelling of predictive technology represents the modelling of deep submicron effects including short-channel behaviour, the saturation of velocity, the leakage currents and the parasitic capacitance. The models make sure that the outcomes of the simulation are similar to real fabrication conditions. The supply voltage is also considered to be in line with the trends in technology scaling and $V_{\text{dd}} = 1.0\text{V}$ in the 45 nm node and $V_{\text{dd}} = 0.9\text{V}$ in the 28 nm node. The values are realistic operating conditions of the present low-power digital systems. Also to be able to bring the same level of performance evaluation, temperature is held to standard room conditions (300 K). Parasitic extraction is also included to consider the interconnect effects to enhance the quality of delay and power estimates. This full simulation environment will allow a realistic test of the proposed design with a realistic operating constraint.

5.2 Test bench Configuration: An efficient and versatile testbench is established to examine the operation of the suggested CCFF in the changing conditions. The input stimulus is made such that it produces pseudo-random data sequences with known transition probabilities and thus systematic analysis of the conditional capture mechanism is possible. The testbench is able to recreate the behavior of the flip-flop in a variety of real-life conditions by adjusting the probability of the transitions between low activity ($P=0.1$) and high activity ($P=0.9$). In order to simulate realistic loading conditions a capacitive load of 10 fF is added to the node of the output of the circuit, the effects of interconnect and fan-out are usually seen in integrated circuits. The clock signal is created using a 50 per cent duty cycle and the frequency range of operation is changed to 100 MHz to 1 GHz which is analysed to study frequency scalability. Caution is observed to provide appropriate setup and hold time as well as not to experience metastability problems during simulation. Measurement probes on instantaneous and average power consumption, timing characteristics are also found in the testbench. This detailed design allows proper evaluation of both functional and performance issues of the proposed design.

5.3 Performance Metrics: The activity of the proposed CCFF is measured by such important indicators as energy efficiency and operational speed. The main parameters that will be taken into consideration are average power consumption, propagation delay and power-delay product (PDP). Transient simulation analysis is used to compute the average power consumption (P_{avg}) with several clock cycles to be sure that both the dynamic and short-circuit power components are accurately represented. Propagation delay (t_{pd}) is defined as the difference between the 50% points in the input and output signals which is a conventional method of delay measurement in digital circuits. This is a technology-independent non-volatile way of measuring circuit speed. To analyse the trade-off between power and performance power-delay product is obtained by taking the formula:

$$\text{PDP} = P_{\text{avg}} \times t_{\text{pd}}$$

The PDP is the amount of energy per switching cycle and is a very broad measure of circuit efficiency. The smaller the PDP values the higher the energy-performance balance, which is essential in the design of low-power VLSI. Besides these main measurements, waveform integrity and glitch behavior are also monitored in order to assure sound operation of the circuit.

5.4 Comparative Evaluation: In order to justify the efficiency of the suggested CCFF, a more complex comparative study is conducted with respect to traditional master slave flip-flops (MSFF) and pulse triggered flip-flops (P-FF). The designs are all applied on the same technology parameters, supply voltages and loading conditions so that a fair and unbiased comparison is made. This standardized evaluation system presents the opportunity to compare unambiguously the improvement of power consumption, delay, and energy efficiency. Besides, Monte Carlo simulations are performed to understand how variations in the process affect the performance of the circuit. The differences in the most important parameters like threshold voltage, channel length, and oxide thickness are added to make simulation of fabrication uncertainties. The findings show that the proposed CCFF has steady operation and minimum variation of power and delay, thus a high robustness. Statistical analysis proves that design is not sensitive to process variations and thus can be used in large scale integration. On the whole, the comparative analysis proves that the proposed CCFF performs better than traditional designs regarding the power efficiency, besides having competitive timing and high reliability, which is why it should be considered in next-generation low-power VLSI systems.

6. Results and Discussion

6.1 Power Consumption Analysis: The transistor level simulations of the proposed Conditional Capture Flip-Flop (CCFF) were thoroughly conducted to create a fair comparison with conventional designs because the power consumption properties of the proposed design were determined at the same operating conditions. As the findings clearly indicate, the CCFF is able to achieve significant dynamic power savings because of its capability to eliminate unwanted switching activity. The proposed design operates at 500 MHz and consumes 12.8 μW in 45 nm CMOS technology compared to the two established designs, master-slave flip-flop (MSFF) and pulse-triggered flip-flop (P-FF) that consume 21.6 μW and 18.3 μW at 500MHz, respectively. This is equal to a 40-50 % drop in power which is significant to the optimization of sequential circuit. The power savings that have been observed can be directly attributed to the conditional capture mechanism, which literally reduces the switching activity factor since it allows internal transitions only in case of input data change. On the standard designs, the clock signal is constantly driving internal nodes no matter what happens to data, charging and discharging internal capacitive loads redundantly. The CCFF on the other hand reduces this behavior by blocking the clock on input transition detection. The result is that not only is the dynamic switching power reduced but also short circuit power due to the simultaneous conduction of pull-up and pull-down networks reduced. Moreover, the decrease in the effective capacitance that happens as a result of conditional clock gating is an added source of power savings. Another effect of the design is that glitch-induced transitions are also suppressed, a cause of energy loss in high-speed circuits. Fig. 3 reveals that the proposed CCFF is always very successful when compared to the existing architectures of flip-flops, which proves that it is a suitable low-power architecture to be used in the modern VLSI systems.

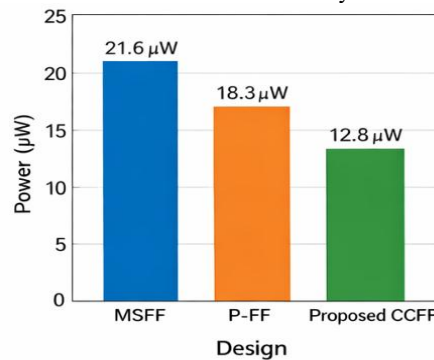


Figure 3: Dynamic Power Comparison

6.2 Delay Performance Evaluation: The propagation delay of the proposed CCFF is considered to make sure that reduction of power does not affect performance deterioration. Simulation findings show that the CCFF has a propagation delay of 92 ps, as compared to 85 ps in case of the MSFF, and 98 ps in case of the P-FF. The trade off between speed and power efficiency is a balanced approach in that though the delay of the proposed design is slightly greater than the delay of the MSFF, it is much less than the delay of the pulse-triggered design. This delay increment is mainly explained by the addition of the transition detecting logic that adds another logic step in the signal path. This overhead is however reduced with optimized transistor sizing and effective implementation of logic. Additionally, the difference in the delay between the various conditions of operation is small which suggests constant timing behavior. However, it should be remembered that the delay penalty is insignificant as far as the power consumption reduction is very significant. This kind of trade-off can be quite desirable in high-performance and low-power applications, where the design of energy efficiency is a factor of critical concern. The CCFF has a good timing aspect up to higher frequencies thus its applicability in high-speed digital systems.

6.3 Power-Delay Product Analysis:

A measure of overall energy efficiency of digital circuits is the power-delay product (PDP) which is a measure of the trade-off between the speed and power consumption. The observed PDP of the proposed CCFF is also much better (1.18 fJ) compared to 1.84 fJ of MSFF and 1.79 fJ of P-FF. This is a saving of about 35-40 %, and this shows how much superior the proposed design is in terms of energy consumption. This is mainly due to the fact that PDP is reduced by the large reduction in the dynamic power consumption, yet competitive delay performance is retained. The CCFF is a superior design compared to conventional designs, in which the trends of power and delay are frequently in conflict, and selectively decreases switching activity without additional delay overhead. As shown in Fig. 4, the proposed design has lower values of PDP in all operating conditions, thereby making it very convenient in cases of limited energy supply. The enhanced PDP also means lower energy per switching event which is especially useful in battery-powered and energy-harvesting systems.

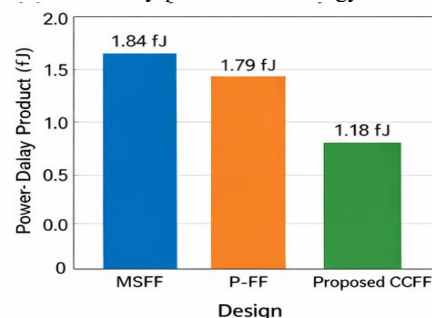


Figure 4: Power-Delay Product (PDP) Comparison

6.4 Impact of Switching Activity and Frequency

Input switching activity is also a key factor in the effectiveness of the proposed CCFF and vital in defining dynamic power consumption. The results of simulation show that with low transition probabilities the CCFF can realize power savings that are more than 50 % and thus is effective when the data activity is less frequent. It is especially applicable in the control logic area, memory elements, and embedded systems, where transitions of an input are infrequent. The power savings also reduce progressively as the switching activity goes up but the proposed design still beats the usage of conventional flip-flops because of the natural capability to remove unnecessary clock-driven transitions. The correlation between switching activity and the power consumption puts emphasis on the versatility of the CCFF to varying workload conditions. Along with the study of switching activity, the effect of the operating frequency is also examined. As the dynamic power consumption is directly proportional to the frequency, high operating frequencies generally lead to high power dissipation. The CCFF is however more scalable since the switching activity reduction is enhanced at high frequencies. The proposed design, as indicated in Fig. 5, has a constant power advantage over the wide range of frequency, which also verifies its applicability in high-frequency and high-performance applications.

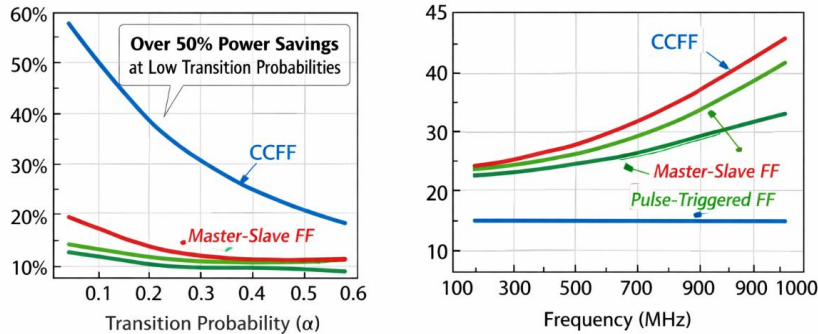


Figure 5: Power vs Frequency Analysis

6.5 Robustness and Reliability

The strength of the suggested CCFF is tested by the use of large Monte Carlo simulation in order to consider the process variations such as the variation in the threshold voltage, variation in the length of the channel and variation in the oxide thickness. The findings show that, the CCFF has a consistent operation with a slight change in the power consumption and propagation delay and therefore it is highly resilient to manufacturing uncertainties. The conditional capture process automatically minimizes internal switching activity that minimizes glitch propagation and short-circuit currents. This helps in increasing signal integrity and decreasing the noise susceptibility, which is extremely crucial in deep submicron technologies. Also, the decrease in switching activity will decrease thermal stress and increase the device reliability in case of long-term operation. The design is also characterized by the same performance under varying voltage and temperature environments, which further proves its relevance to practical applications. The philosophy of low power use, deterministic timing behavior, and reliability offered by the proposed CCFF represents a perfect fit to be used in the current low-power VLSI systems, such as Internet of Things gadgets, wearable electronics, and portable computer systems.

7. Conclusion

This paper has introduced a new Conditional Capture Flip-Flop (CCFF) architecture sought to lower the dynamic power drawing in low-power VLSI systems. Using a transition-conscious control scheme, the inferred design can be used to reduce the amount of switching that is not required by internal nodes, which is a significant source of energy dissipation in standard sequential circuits. The data transition detection and conditional clock gating have been integrated to allow the selective activation of the storage element, and as a result, unnecessary clock-driven transitions have been minimized, but without functional correctness. The results of the mathematical modeling and simulation confirm the usefulness of the provided approach. The CCFF gives very high power savings of up to 40-50 % over conventional master slave and pulse-triggered flip-flops with competitive delay performance. Moreover, the increased value of the power-delay product emphasizes the energy efficiency of the design, which makes it very anatomically appropriate to the current modern developments like IoT devices, wearable electronics, and battery-powered embedded systems. It has also a high robustness to variation in the process design that makes it reliable in operation in deep submicron technologies. The next development of the work can be carried out in the direction of the extension of the proposed conditional capture mechanism to more complicated sequential components such as registers and memory arrays. Also, it can be further energy efficient by integrating with multi-bit flip-flop architecture, and adaptive voltage scaling methods. Looking at layout-level optimization and silicon validation will be also important to the real world deployment. Another potential avenue of future study of the ultra-low-power VLSI design is the addition of machine learning methods of adaptive switching prediction.

References

- [1]. Chandrakasan AP, Brodersen RW. Low power CMOS digital design. IEEE J Solid-State Circuits. 1995;27(4):473-484. doi:10.1109/4.289848
- [2]. Kong BS, Kim SS, Jun YH. Conditional-capture flip-flop for statistical power reduction. IEEE J Solid-State Circuits. 2001;36(8):1263-1271. doi:10.1109/4.933463
- [3]. Teh CK, Fujita T, Hara H, Sakurai T. Conditional data mapping flip-flops for low-power design. IEEE Trans VLSI Syst. 2006;14(6):631-640. doi:10.1109/TVLSI.2006.876124
- [4]. Strollo AGM, De Caro D, Napoli E. Low-power flip-flop with clock gating. Electron Lett. 2005;41(21):1235-1236. doi:10.1049/el:20052774
- [5]. Nedovic N, Aleksic M. Conditional precharge techniques for power reduction. IEEE Trans Circuits Syst II. 2001;48(9):803-807. doi:10.1109/82.954499
- [6]. Llopis R, Sachdev M. Low power testable flip-flops. IEEE J Solid-State Circuits. 1996;31(3):369-376. doi:10.1109/4.494195
- [7]. Kim J, Roy K. Double-edge triggered flip-flop for low power. IEEE Trans VLSI Syst. 2002;10(3):339-346. doi:10.1109/TVLSI.2002.1017994
- [8]. Alioto M. Ultra-low power VLSI circuit design. Springer. 2012. doi:10.1007/978-1-4614-2069-7
- [9]. Rabaey JM, Chandrakasan AP, Nikolic B. Digital integrated circuits: A design perspective. Prentice Hall. 2003. doi:10.5555/861369
- [10]. Weste NHE, Harris D. CMOS VLSI design: A circuits and systems perspective. Addison-Wesley. 2011. doi:10.5555/2027745
- [11]. Frank DJ, Dennard RH, Nowak E, et al. Device scaling limits of Si MOSFETs. Proc IEEE. 2001;89(3):259-288. doi:10.1109/5.915374
- [12]. Roy K, Mukhopadhyay S, Mahmoodi-Meimand H. Leakage current mechanisms and reduction techniques. Proc IEEE. 2003;91(2):305-327. doi:10.1109/JPROC.2002.808156
- [13]. Calhoun BH, Chandrakasan AP. Ultra-dynamic voltage scaling. IEEE J Solid-State Circuits. 2006;41(11):2380-2390. doi:10.1109/JSSC.2006.884874
- [14]. Pedram M. Power minimization in IC design: Principles and applications. ACM Trans Des Autom Electron Syst. 1996;1(1):3-56. doi:10.1145/227999.228005
- [15]. Benini L, De Micheli G. System-level power optimization. IEEE Trans VLSI Syst. 2000;8(3):299-316. doi:10.1109/92.845896
- [16]. Zhang M, Gu J, Chang CH. Low-power pulse-triggered flip-flops. IEEE Trans VLSI Syst. 2010;18(1):107-111. doi:10.1109/TVLSI.2008.2000458
- [17]. Lin JF, Hwang YC, Sheu MH, Ho CC. Low-power latch design with clock gating. IEEE Trans VLSI Syst. 2009;17(8):1142-1146. doi:10.1109/TVLSI.2008.2008873
- [18]. Baek K, Kim H, Lee J. Conditional clocking for low-power flip-flops. IEEE J Solid-State Circuits. 2003;38(5):870-873. doi:10.1109/JSSC.2003.811978
- [19]. Veendrick HJM. Short-circuit power dissipation of static CMOS. IEEE J Solid-State Circuits. 1984;19(4):468-473. doi:10.1109/JSSC.1984.1052183
- [20]. Friedmann EG. Clock distribution networks in synchronous digital systems. Proc IEEE. 2001;89(5):665-692. doi:10.1109/5.929649